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Application No.	09/626,535
Filing Date	July 27, 2000
First Named Inventor	Donald F. Hooper
Art Unit	2155
Examiner Name	ENG, David Y
Total Number of Pages in This Submission	Attorney Docket Number: 42390P7876X

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
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  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
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- ☐ Proprietary Information
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Mark C. Van Ness, Reg. No. 39,865 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	August 3, 2005

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Katherine Jennings		
Signature	Katherine Jennings	Date	August 3, 2005

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Mark C. Van Ness	Registration No. (Attorney/Agent)	39,865	Telephone	(503) 439-8778
Signature				Date	08/03/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	: Hooper, et. al.	Art Unit	: 2155
Serial No.	: 09/626,535	Examiner	: Eng, David Y
Filed	: 7/27/2000	Assignee	: Intel Corporation
Title	: MULTI-THREADED SCHEDULED RECEIVE FOR FAST NETWORK PORT DATA		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

(i) Real Party in Interest

The real party in interest in this appeal is Intel Corporation, a Delaware corporation having a principal place of business at 2200 Mission College Blvd, Santa Clara, CA 95052. Intel is the assignee of the entire right, title, and interest in the above-noted application.

(ii) Related Appeals and Interferences

A notice of appeal was filed on 4/22/2005 for U.S. serial no. 09/475,614, entitled "Method and Apparatus for Control of Receive Data". The corresponding appeal brief for that application was filed on 7/22/2005. No decision has been rendered by the Board.

(iii) Status of Claims

Claims 1 and 3-20 are pending and being appealed with claims 1, 7, and 15 being independent.

Claim 2 was previously cancelled.

(iv) Status of Amendments

No amendments were filed after the final rejection mailed on 03/29/2005.

(v) Summary of Claimed Subject Matter

The independent claims recite subject matter relating to a processor having multiple programmable multi-threaded engines. For example, FIG. 1 depicts a processor 12 including multiple programmable microengines 22. Each of the microengines provides multiple program threads (page. 4, lines 7-9). The processor 12 processes network packets received from one or more media access control devices 30, 31 (page 5, lines 13-page 6, line 2). Different threads provided by the microengines process the network packets (e.g., page 23, lines 7-11). In particular, as recited by the

independent claims, different portions/blocks of a given packet are processed by different threads in specific ways.

For example, as recited in claim 1, a second thread may be scheduled to process a second incoming block of data within a network packet prior to a first thread completing processing of a first block of data within the packet. For instance, as shown in FIG. 12, thread "y" 304 is scheduled to process a second block of a packet's data before thread "x" 303 completes processing of a first block of the packet's data.

As another example, as recited in claim 7, a second thread can process a second portion of a network packet simultaneously with a first thread processing a first portion of the network packet. For instance, as shown in FIG. 12, while thread "x" 303 processes a first portion of a packet, thread "y" 304 processes a second portion.

Finally, as recited in claim 15, a first thread and a second thread that do not time share can process respective first and second portions of a data packet. For example, threads "x" 303, "y" 304, and "z" 305 can be executed in different microengines but still process different portions of the same packet (page 23, line 24-25). The operation of the threads can be caused by computer-executable instructions executed by the processor (page 6, lines 9-12).

(vi) Grounds of Rejection to be Reviewed on Appeal

Claims 1 and 3-20 are rejected as being unpatentable over Kirk (USP 4,709,347) in view of Mohamed (USP 6,366,998)

(vii) Arguments

(a) Legal Standard of Obviousness

"It is well established that the burden is on the PTO to establish a prima facie showing of obviousness, *In re Fritsch*, 972 F.2d. 1260, 23 U.S.P.Q.2d 1780 (C.C.P.A., 1972)."

"It is well established that there must be some logical reason apparent from the evidence or record to justify combination or modification of references. *In re Regal*, 526 F.2d 1399 188, U.S.P.Q.2d 136 (C.C.P.A. 1975). In addition, even if all of the elements of claims are disclosed in various prior art references, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill in the art would have been prompted to combine the teachings of the references to arrive at the claimed invention. Id. Even if the cited references show the various elements suggested by the Examiner in order to support a conclusion that it would have been obvious to combine the cited references, the references must either expressly or impliedly suggest the claimed combination or the Examiner must present a convincing line of reasoning as to why one skilled in the art would have found the claimed invention obvious in light of the teachings of the references. *Ex Parte Clapp*, 227 U.S.P.Q.2d 972, 973 (Board. Pat. App. & Inf. 985)."

"The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon*, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

> Although the Commissioner suggests that [the structure in the primary prior art reference] could readily be modified to form the [claimed] structure, "[t]he mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Laskowski*, 10 U.S.P.Q. 2d 1397, 1398 (Fed. Cir. 1989).

"The claimed invention must be considered as a whole, and the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination." *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 U.S.P.Q. 481, 488 (Fed. Cir. 1984).

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention,

> absent some teaching or suggestion supporting the combination. Under Section 103, teachings of references can be combined only if there is some suggestion or incentive to do so. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984) (emphasis in original, footnotes omitted).

"The critical inquiry is whether 'there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'" *Fromson v. Advance Offset Plate, Inc.*, 225 U.S.P.Q. 26, 31 (Fed. Cir. 1985).

(b) Independent Claim 1

In the Office Action mailed 9/28/2004, the Examiner rejected claim 1 as unpatentable over Kirk in view of Mohamed. In making the rejection, the Examiner made the following statement regarding the teachings of Kirk:

> With respect to claim 1, 7, 15, Kirk teaches a method of processing network data (see Local Area Network 10 in Figure 1 of Kirk and lines 2-11 of column 4), in a processor (MOD) having multiple programmable multi-threaded (bit-slice) engines (see programmable micro-engine 18-04 in BIU of Figure 2 and lines 23-39 of column 4) integrated within the processor, the method comprising:
>
> scheduling a first thread provided by the multiple programmable multi-threaded engines (see programmable micro-engines)integrated within the processor to process a first incoming block of data within a network packet (packet is inherent in network system) received at port (see transceiver 18-04 of Fig. 2) of a media access control device.

(page 2, Office Action mailed 9/28/2004).

Applicants continue to disagree that Kirk teaches a multi-threaded engine. That is, the Examiner has equated Kirk's bit-slice architecture with a multi-threaded engine. However, as also indicated in the application incorporated by reference into Kirk (see col. 5, lines 2-4 of U.S. Pat. No. 4,556,974), the bit-slice architecture in Kirk refers to a type of ALU (Arithmetic Logic Unit) architecture where a larger ALU (e.g., an 8-bit ALU) is formed by combining narrower ALUs (e.g., 1-bit ALUs). Each of the narrower ALUs is known as a "bit-slice". However, an ALU bit-slice is not the same thing as a thread. Thus, the microengine 18-04 of Kirk is not a multi-threaded engine.

The Examiner then proposes modifying the BIU of Kirk to include multiple microengines 18-04 instead of a single one based on the teachings of Mohamed. The Examiner stated:

> It appears that Kirk has only one (micro) engine instead of plurality. See Figures 1, 2 and 8 and the corresponding description in Mohamed. Mohamed teaches a processor having a plurality of DPUs and a scheduler. Each DPU provides a thread for processing incoming data. Each of the threads is scheduled by the scheduler to process simultaneously respective incoming data streams. From the teaching of Mohamed, it would have been obvious to a person of ordinary skill in the art to employ more than one engine of Kirk so that more than one thread of incoming data can be processed simultaneously.

(pages 2-3, Office Action mailed 9/28/2004).

Assuming for the sake of argument that one of skill in the art would modify Kirk, based on the teachings of Mohamed, to include multiple microengines 18-04 instead of a single microengine 18-04, the resulting combination would still not provide the recited subject matter. That is, since the microengine 18-04 of Kirk is not multi-threaded, modifying the BIU of Kirk to include multiple copies of the Kirk microengine 18-04 would still not yield a processor having multiple multi-threaded engines or even a single multi-threaded engine for that matter. Additionally, assuming for the sake of argument, that there were some reason to modify Kirk to include multiple multi-threaded engines, there is nothing in Kirk or Mohamed that teaches that a given network packet received by a media access control device should be processed by more than one thread, let alone in the manner recited by claim 1 (i.e., scheduling a second thread to process a second

incoming block of data within a network packet prior to a first thread completing processing of the first incoming block of data).

Further, Applicants disagree that, based on the teachings of Mohamed, that it would have been obvious to a person of one skill in the art to employ more than one engine of Kirk "so that more than one thread of incoming data can be processed simultaneously". In particular, the Applicants do not understand the Examiner's statement regarding "threads of incoming data". Claim 1 does not recite "threads of incoming data" nor does the specification describe data as being "threaded". Additionally, in proposing this combination, the Examiner states that each DPU provides a thread for incoming data, however, the term "thread" is not used in Mohamed, nor does the Examiner state what is being deemed a thread in Mohamed.

Finally, in replying to the Applicants arguments, the Examiner repeatedly replied by stating that a DPU in Mohamed is a thread engine (page 3, Office Action Mailed 3/29/05; sheet 2, Advisory Action mailed 5/31/05). Again, Mohamed does not use the term "thread" nor does the Examiner specifically state what is considered to be a thread in Mohamed. Additionally, even if the Examiner's position is adopted for the sake of argument, Applicants do not understand how this would change the analysis. That is, the Examiner would still have not proposed a combination that would provide multiple multi-threaded engines that process a network packet as recited by claim 1.

(c) Independent Claim 7

Like claim 1, claim 7 recites multiple programmable multi-threaded engines. Claim 7, however, recites processing a second portion of the network packet using a second thread simultaneously with the processing of a first portion of the network packet using a first thread.

Applicants' argument regarding claim 7 is similar to that described above. That is, neither Kirk nor Mohamed teach multiple programmable multi-threaded engines, nor do either Kirk or Mohamed teach processing a network packet using more than one thread. Given that neither Kirk nor Mohamed teach processing a network packet using

more than one thread, neither Kirk nor Mohamed, alone or in combination describe or suggest processing a second portion of the network packet using a second thread simultaneously with the processing of a first portion of the network packet using a first thread.

(d) Independent Claim 15

Like claim 1, claim 15 recites multiple programmable multi-threaded engines. Claim 15, however, recites that a first thread and a second thread that do not time share can process respective first and second portion of the data packet.

Applicants' argument regarding claim 15 is similar to that described above. That is, neither Kirk nor Mohamed teach multiple multi-threaded programmable engines, nor do either Kirk or Mohamed teach processing a network packet using more than one thread. Given that neither Kirk nor Mohamed teach processing a network packet using more than one thread, neither Kirk nor Mohamed, alone or in combination describe or suggest that a first thread and a second thread that do not time share can process respective first and second portion of the data packet.

(e) Dependent Claim 10

Dependent claim 10 recites that the first and second threads recited by claim 7 time share with one another. In rejecting a different claim (claim 8) the Examiner stated:

> With respect to claim 8, there is no time sharing in Kirk or Mohamed.

(page 3, Office Action mailed 9/28/04).

Thus, the rejection of claim 10 which recites that the threads **do** time share is inconsistent with the Examiner's position regarding claim 8. The Examiner's did comment on claim 10 as follows:

> With respect to claims 10, 11 and 14, the wherein clauses merely state the result of the limitations recited in parent claim 7. The clauses therefore add nothing to the patentability or substance of the claims.

(page 3, Office Action mailed 9/28/04).

First, Applicants disagree that claim 10 is a result of the limitations of claim 7. Second, Applicants are unaware of legal support for the Examiner's position that the limitations of claim 10 should not be given patentable weight. Based on the Examiner's stated position that neither Kirk nor Mohamed describe time sharing and the failure to give weight to the limitations of claim 10, Applicant's request withdrawal of the rejection of dependent claim 10.

(viii) Claims Appendix

1. A method of processing network data in a processor having multiple programmable multi-threaded engines integrated within the processor, the method comprising:

scheduling a first thread provided by the multiple programmable multi-threaded engines integrated within the processor to process a first incoming block of data within a network packet received at port of a media access control device ; and

scheduling a second thread provided by the multiple programmable multi-threaded engines integrated within the processor to process a second incoming block of data within the network packet prior to the first thread completing processing of the first incoming block of data.

3. The method of claim 1 further comprising:
saving state information by the first thread; and
retrieving the state information by the second thread.

4. The method of claim 3, wherein the state information includes a pointer into a memory indicating where to move the first and second incoming blocks of data.

5. The method of claim 4 further comprising:
storing data to memory in a sequential ordering based on the state information.

6. The method of claim 5 further comprising:
providing the state information to transmit circuitry.

7. A method of processing a network packet received over a network at a processor having multiple programmable multi-threaded engines integrated within the processor, the method comprising:

processing a first portion of the network packet received at port of a media access control device using a first thread provided by the multiple programmable multi-threaded engines integrated within the processor; and

simultaneously processing a second portion of the network packet using a second thread provided by the multiple programmable multi-threaded engines integrated within the processor.

8. The method of claim 7 wherein the first thread and the second thread do not time share processing with one another.

9. The method of claim 8 wherein the first thread and the second thread operate out of different ones of the multiple multi-threaded engines integrated within the processor.

10. The method of claim 7 wherein the first thread and the second thread time share processing with one another.

11. The method of claim 10 wherein the first thread and the second thread operate out of a common one of the multiple multi-threaded engines integrated within the processor.

12. The method of claim 7 further comprising:

simultaneously with processing the first portion and the second portion of the network packet, processing a third portion of the network packet using a third thread.

13. The method of claim 12 wherein the first thread, the second thread, and the third thread run the same code.

14. The method of claim 13 wherein the first thread, the second thread, and the third thread do not time share processing with one another.

15. An article comprising a computer-readable medium which store computer-executable instructions for receiving data from a plurality of ports, the instructions causing a processor having multiple programmable multi-threaded engines integrated within the processor, the method to:

process a first portion of a data packet using a first thread provided by the multiple programmable multi-threaded engines integrated within the processor; and

process a second portion of the data packet using a second thread provided by the multiple programmable multi-threaded engines integrated within the processor, wherein there is no time sharing between the first thread and the second thread.

16. The article of claim 15, the article further comprises instructions to:

save state information of the first thread; and

restore the state information by the second thread.

17. The article of claim 16, the article further comprises instructions to:

provide the state information to transmit circuitry when an end of packet is detected by a subsequent thread.

18. The method of claim 1, wherein the network packet comprises an Ethernet packet.

19. The method of claim 1, further comprising monitoring the port of the media access control device for received data.

20. The method of claim 1, wherein the processing comprises:

parsing the header of the received network packet;

performing a lookup based on the parsing; and

enqueuing an entry in a transmit queue for the network packet based on the performed lookup.

Respectfully submitted,

Date: August 3, 2005

Mark C. Van Ness
Reg. No.: 39,865

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box [illegible], VA 22313 on:

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Katherine Jennings
Name of Person Mailing Correspondence

Katherine Jennings August 3, 2005
Signature Date